In re Patent Application of:
OM ET AL.
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In the Claims:

1. (Currently amended) A digital logic system comprising:

a reset input for receiving a reset signal;

a clock input for receiving an externally generated main clock signal;

an ancillary clock generator for generating an ancillary clock signal independent of the externally generated main clock signal and having short term frequency stability in relation to an expected duration of a system reset phase;

at least one functional circuit;

a clock selection multiplexer having a first input for receiving the externally generated main clock signal, a second input for receiving the ~~internally generated~~ ancillary clock signal, and an output for providing the externally generated main clock signal or the ~~internally generated~~ ancillary clock signal to said at least one functional circuit; and

a resettable edge-triggered shift register having a first input for receiving the externally generated main clock signal, a second input for receiving the reset signal, and an output connected to said clock selection multiplexer for deselecting the ~~internally generated~~ ancillary clock signal and selecting the externally generated main clock signal after detecting a certain number of edges of the main clock signal following the reset signal.

2. (Original) A digital logic system according to Claim 1, wherein said ancillary clock generator comprises a

ring/RC oscillator.

3. (Original) A digital logic system according to Claim 1, wherein said resettable edge-triggered shift register comprises a plurality of stages for preventing glitches that may be present on the externally generated main clock signal.

4. (Original) A digital logic system according to Claim 1, further comprising a toggle flip-flop between the first input of said resettable edge-triggered shift register and the clock input.

5. (Original) A digital logic system according to Claim 1, wherein a frequency of the ancillary clock signal is less than a frequency of the main clock signal.

6. (Currently amended) A digital logic system comprising:

a reset input for receiving a reset signal;

a clock input for receiving an externally generated main clock signal;

an ancillary clock generator for generating an ancillary clock signal <u>independent of the externally generated main clock signal</u>;

a clock selection multiplexer having a first input for receiving the externally generated main clock signal, a second input for receiving the ~~internally generated~~ ancillary clock signal, and an output for providing the externally generated main clock signal or the ~~internally generated~~ ancillary clock signal; and

a shift register having a first input for receiving the externally generated main clock signal, a second input for receiving the reset signal, and an output connected to said clock selection multiplexer for deselecting the ~~internally generated~~ ancillary clock signal and selecting the externally generated main clock signal after detecting a certain number of edges of the main clock signal following the reset signal.

7. (Original) A digital logic system according to Claim 6, wherein said ancillary clock generator comprises a ring/RC oscillator.

8. (Original) A digital logic system according to Claim 6, wherein said shift register comprises a plurality of stages.

9. (Original) A digital logic system according to Claim 6, further comprising a toggle flip-flop between the first input of said shift register and the clock input.

10. (Original) A digital logic system according to Claim 6, wherein a frequency of the ancillary clock signal is less than a frequency of the main clock signal.

11. (Currently amended) A digital system comprising:

a reset circuit for generating a reset signal;

a main clock generator for generating a main clock signal;

an ancillary clock generator for generating an

ancillary clock signal independent of the externally generated main clock signal;

at least one functional circuit;

a clock selection multiplexer having a first input for receiving the main clock signal, a second input for receiving the ancillary clock signal, and an output for providing the main clock signal or the ancillary clock signal to said at least one functional circuit; and

a resettable edge-triggered shift register having a first input for receiving the main clock signal, a second input for receiving the reset signal, and an output connected to said clock selection multiplexer for deselecting the ancillary clock signal and selecting the main clock signal after detecting a certain number of edges of the main clock signal following the reset signal.

12. (Original) A digital system according to Claim 11, wherein said ancillary clock generator comprises a ring/RC oscillator.

13. (Original) A digital system according to Claim 11, wherein said shift register comprises a plurality of stages.

14. (Original) A digital system according to Claim 11, further comprising a toggle flip-flop between the first input of said shift register and said main clock generator.

15. (Original) A digital system according to Claim 11, wherein a frequency of the ancillary clock signal is less

than a frequency of the main clock signal.

16. (Currently amended) A method for resetting a digital logic system comprising a reset input for receiving a reset signal and a clock input for receiving an externally generated main clock signal, the method comprising:

generating an ancillary clock signal independent of the externally generated main clock signal;

providing the externally generated main clock signal and the ancillary clock signal to respective first and second inputs of a clock selection multiplexer, and providing at an output of the clock selection multiplexer the externally generated main clock signal or the ancillary clock signal to at least one functional circuit; and

providing the externally generated main clock signal and the reset signal to respective first and second inputs of a resettable edge-triggered shift register, and an output of the resettable edge-triggered shift register being connected to the clock selection multiplexer for deselecting the ancillary clock signal and selecting the externally generated main clock signal after the resettable edge-triggered shift register detects a certain number of edges of the main clock signal following the reset signal.

17. (Original) A method according to Claim 16, wherein the ancillary clock generator comprises a ring/RC oscillator.

18. (Original) A method according to Claim 16, wherein the resettable edge-triggered shift register comprises

a plurality of stages.

19. (Original) A method according to Claim 16, wherein the digital logic system further comprises a toggle flip-flop between the first input of the resettable edge-triggered shift register and the clock input.

20. (Original) A method according to Claim 16, wherein a frequency of the ancillary clock signal is less than a frequency of the main clock signal.